REMARKS

Claims 1 - 5 and 7 - 20 were pending in the present application for patent as of the Office Action of June 29, 2004. In the Office Action of June 29, 2004, the examiner rejected claims 1, 2, 7, 8, 11 - 16, and 18 - 20 under 35 U.S.C. 102(a) as being anticipated by Yeivin et al. (WO00/60477), rejected claims 3 - 5 and 17 under 35 U.S.C. 103(a) as being unpatentable over Yeivin et al. in view of U.S. Patent Number 5,761,424, Adams et al., rejected claim 9 under 35 U.S.C. 103(a) as applied to claims 1, 2, 7, 8, 11 - 16, and 18 - 20 above and further in view of U.S. Patent Number 6,530,047, Edwards et al., and rejected claim 10 under 35 U.S.C. 103(a) as applied to claims 1, 2, 7, 8, 11 - 16, and 18 - 20 above and further in view of U.S. Patent Number 6,529,970, Sarpangal and U.S. Patent Number 6,621,834, Scherpbier. The office action was made final.

In the previous office action mailed February 9, 2004, the examiner objected to the specification because there was no "Brief Summary of the Invention", objected to the disclosure because of an informality, and objected to the drawings. The examiner did not mention these objections in the final rejection. Unless notified otherwise, the applicants will assume that these objections were overcome by the applicants in the previous response mailed May 10, 2004.

Claims 1, 2, 7, 8, 11 - 16, and 18 - 20 were rejected under 35 U.S.C. 102(a) as being anticipated by Yeivin et al. In response, the applicants have amended claims 1 and 13 to remove the phrase "to allow a plurality of channel handlers to be logically grouped within the communications handler" and to correct a minor typographical error.

Yeivin et al. discloses a communications controller 111 comprising a scheduler 50, a first DMA 60, a second DMA 160, a first memory bank 70, a first processor 90, an instruction memory bank 130, a second processor 100 and multiple peripherals. These components are all shown in Figure 3 of Yeivin et al. The multiple peripherals are collectively designated as reference 140 and coupled to multiple communications channels 180. Yeivin et al. also discloses first and second buses 113, 114 to which the communications controller is coupled. The peripherals 140, as stated above, comprise a number of individual peripherals. According to page 9, lines 13 to 14, each peripheral is usually tailored to handle one or more communications protocol. Further as explained at lines 21 to 23 on page 8, the multiple peripherals 140 couple the communication controller 111 to the multiple communications channels 180.

In the Office Action of June 29, 2004, the Examiner asserted that the "communication handler" as recited in Claims 1 and 13 is equivalent to the peripherals 140, the scheduler 50 and

the first processor 90 disclosed in Yeivin et al. More precisely, in order to satisfy the programmability aspect of the communications handler recited in Claims 1 and 13, the Examiner seems to have concluded that the equivalent to the communications handler comprises the first processor 90 of Yeivin et al. However, the applicants believe that drawing such a parallel is incorrect. First, to argue that the Yeivin et al. equivalent to the communications handler includes the first processor 90 leaves the control unit 74 of the present application without an equivalent and therefore an inconsistency exists. Second, and more important, even if the equivalence asserted by the examiner were to be correct, the combination of the peripherals 140, the scheduler 50 and the first processor 90 does not perform transformations on the data stream at a bit-level.

The applicants respectfully submit that the examiner has misinterpreted the operation of Yeivin et al. In this respect, Yeivin et al. is directed to communication controllers for use with networking and telecommunications products. In contrast, the application in suit is intended for automotive applications. Consequently, it is sufficient for the apparatus of Yeivin et al. to operate on data streams at the byte, or word, level.

While the examiner has cited the paragraph bridging pages 9 and 10 of Yeivin et al. as disclosing programming on a bit level, particularly the last few lines, this paragraph simply explains the role of the peripherals 140. In relation to the peripherals 140, there are two important points to note. First, the peripherals are not themselves programmable; they are simply "tailored" to handle one or more communications protocols (as explained at lines 13 to 14 of page 9). Secondly, one of the functions of the peripherals 140 is to convert the format of the data stream from parallel data to a stream of (serial) bits. Support for this assertion can be found at lines 25 to 28 on page 9. Hence, of the peripherals 140, the scheduler 50 and the first processor 90, the only element that is programmable is the first processor 90. However, data processed by the processor 90 is "prepared" prior to processing by the first processor 90. More precisely, when processed, the data processed by the first processor is in blocks of 8 bits, i.e. a byte or word. Therefore, it is submitted that the equivalent in Yeivin et al. to the communications handler does not perform transformations on the data stream at a bit-level, rather at a byte level. The reference to a stream of single bits in Yeivin et al. is simply in connection with the act of parallel-to-serial conversion for peripherals that deal with serial communications protocols and as such need to do something with the data bytes received from the first processor 90 and similarly need to prepare received single bit streams prior to processing by the first processor 90. Page 9, lines 25 to 28, states: "Peripherals which deal with serial

communications protocols usually are comprised from parallel to serial converters, such as shift register, which receive form a communication channel a serial data bit stream, and convert the bit stream into a set of multiple bit words, to be sent to the first processor 90." The applicants assert that if a serial-to-parallel data conversion is being carried out prior to the data reaching the first processor 90, then bytes as opposed to bits are being processed by the first processor 90.

Further, the specification makes references to "words" in relation to the first processor 90, for example at lines 14 to 17 on page 24 states: "During step 1022, first processor 90 fetches BF(k), according to DP(k), which was fetched previously. TMP(k) gets the value of PT(k), because first processor 90 will start to write data words received from CC(k) to the beginning of BF(k)." Likewise, page 11, lines 23 to 28 gives further support to the applicants' assertion that processor 90 operates on words and not bits.

The ability of the communications handler to be programmable to perform transformations of the bit stream at a bit-level is particularly advantageous in the field of communications for automotive applications, because the communications handler can be programmed to handle a far greater number of protocols than the apparatus of Yeivin et al. In particular, Yeivin et al. is constrained in the protocols that can be supported by the non-programmable peripherals 140. Consequently, while the apparatus of Yeivin et al. can be extended to support byte-based Ethernet or ISDN protocols using an existing DLC peripheral, it is not capable of supporting automotive protocols such as LIN, CAN and Flexray, due to the inflexibility of the peripherals 140 in combination with the first processor 90 to process data at the bit-level.

Therefore, the applicants believe that independent claims 1 and 13, as amended herein, are allowable over Yeivin et al. The applicants believe that the comments above regarding the rejection of claims 1 and 13 also apply to the rejection of claims 2, 7, 8, 11, 12, 14- 16, and 18 - 20, and that claims 2, 7, 8, 11, 12, 14- 16, and 18 - 20 are allowable over Yeivin et al.

Claims 3 - 5 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin et al. in view of Adams et al. Claim 9 was rejected under 35 U.S.C. 103(a) as applied to claims 1, 2, 7, 8, 11 - 16, and 18 - 20 above and further in view of Edwards et al. Claim 10 was rejected under 35 U.S.C. 103(a) as applied to claims 1, 2, 7, 8, 11 - 16, and 18 - 20 above and further in view of Sarpangal and Scherpbier. The applicants believe that the comments above regarding the rejection of claims 1 and 13 also applies to the rejection of claims 3 - 5, 9, 10, and 17, and that claims 3 - 5, 9, 10, and 17 allowable over the cited art.

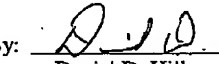
No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed June 29, 2004, the applicants respectfully request the reconsideration and allowance of claims 1 - 5 and 7 - 20; thereby placing the application in condition for allowance.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Customer Number SC0897EM

By: 

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